

A STUDY OF 0201'S AND TOMBSTONING IN LEAD-FREE SYSTEMS

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ABSTRACT

Tombstoning, the phenomena where a chip component stands up on one end during the reflow cycle, is well-documented and understood in tin-lead systems. It is reported to occur more frequently in lead-free systems, and smaller components are at greater risk than larger ones.

A comprehensive DOE was undertaken to characterize tombstoning of 0201 components in different metallurgical solder systems. Factors included pad geometry, board finish, stencil geometry, solder paste type, print and placement offsets, and reflow profile and atmosphere. The experiment was divided into two phases; the results of Phase 1 are analyzed and reviewed.

KEY WORDS: Lead-free, miniaturization, tombstoning, reflow, 0201 components

INTRODUCTION

Tombstoning is a defect mode that has caused yield fallout since the very beginning of SMT assembly. Also known as “drawbridging” or “the Manhattan effect,” it is the phenomena where a chip component seems to stand up on its end during the reflow soldering process.

The mechanics of tombstoning are based on the wetting forces of molten solder and the mass and geometry of the component. If the solder paste under one termination melts and starts wetting to the termination before the other side does, the force applied by the wetting action can pull that component up on its end. Typically, the smaller and lighter the component is, the more susceptible it is to tombstoning.

Factors in tombstoning can be classified into two main categories: design-related and process-related. Design-related factors would include pad design, pad definition

(mask or metal), thermal balance between pads or unfilled microvias in the pads. Process-related factors are numerous, and often difficult to quantify. Many DOEs have been performed and published on the topic, often focusing on best practices for both design and assembly.

Most 0201 assembly processes were optimized prior to the transition to lead-free processing. The increasing production of lead-free products and the tighter process windows associated with lead-free now dictate a reassessment of the key parameters that can affect tombstone formation.

EXPERIMENTAL DESIGN

After review of previously published studies and high-volume production experiences, a listing of factors that can influence tombstone defects resulted in 49 potential parameters. The investigators then used a C&E Matrix approach (rating influence 0, 3 or 9) to identify the following 12 parameters as the most influential:

- Padstacks. This includes pad sizes and spacing between pads. All pads were non-solder mask defined (NSMD), and did not have solder mask between the pads. Four sizes were considered. Three are considered public domain; the fourth is considered proprietary.
- Solder Paste Volume. Stencil apertures were designed at 70% and 100% area of each pad size. 70% area represents the least acceptable transfer efficiency; 100% area represents the best possible transfer efficiency. For the feature sizes used in this study, apertures designed at 70% released about 50% of the paste from the apertures, and apertures designed at 100% released about 60%. The transfer efficiencies vary with each solder paste and the different apertures' area ratios.

- Print offsets. To simulate alignment error, stencil apertures were designed at nominal pad position and with 0.1mm (4 mil) offsets in both X and Y directions, for a total of four combinations: (0,0; 0,0.1; 0.1,0.1; and 0.1,0.1)
- Component type. Both resistors and capacitors were used to capture the effects of component height and number of sides per termination.
- Orientation. Components were mounted at both 0 and 90 degrees.
- Reflow profile. Straight ramp and high soak profiles were used.
- Reflow atmosphere. Air and 100 ppm N2 atmospheres were applied in the soldering cycles.
- Placement offset. Components were placed at two positions: their nominal 0, 0 (CAD) position, and a 0.1, 0.1mm (4 mil) offset in both X and Y concurrently.
- Solder paste. In Phase 1 of the study, three solder pastes were used: no-clean SnPb, no-clean SAC305, and water washable SAC305. In Phase 2, the number of pastes was expanded to seven.
- PWB final finish. In Phase 1, organic solderability preservative (OSP) was used. In Phase 2, both OSP and electroless nickel-immersion gold (ENIG) finishes were used.

The experiment was partitioned into two phases. The experimental matrix for Phase 1 is shown in Table 1.

Final DOE Phase 1					
	Levels	A	B	C	D
Padstack	4				
paste volume	2	100	70		
paste off x	2	0	0.1		
paste off y	2	0	0.1		
comp type	2	R	C		
rotation	2	0	90		
	128	Combinations			
	6400	Parts Placed			
Profile	2	HS	SR		
Atmosphere	2	Air	N2		
Place off x		0	0.1		
Place off y	2	0	0.1		
Place off theta	1	0			
	8				
paste	3	NC-SnPb	WS-SAC305	NC-SAC305	
boards	24				
Replication *2	48				
Parts Placed	307200				

Table 1. DOE Phase 1 Design Matrix

The factors listed in the top portion of Table 1 were designed into the test vehicle shown in Figure 1. The factors in the bottom half of the table were varied during the assembly process.

Test Vehicle

The test vehicle shown in Figure 1 contained 48 individual test cells. Four different pad designs were used, each appearing twelve times on the test vehicle, six times per row of cells on two rows. Each cell had 50 resistors and 50 capacitors oriented at both 0 and 90 degrees for a total of

200 per block, as shown in Figure 2. Eight cells per padstack were assembled per board, for a total of 1600 placements per padstack per board. In phase 1, all four padstacks were used, resulting in 6400 components placements per board.

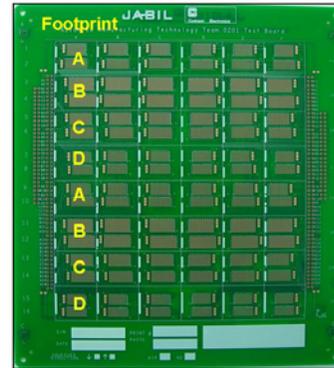


Figure 1. 0201 Test Board Layout. Each row has six test cells. Eight rows duplicate four footprints two times.

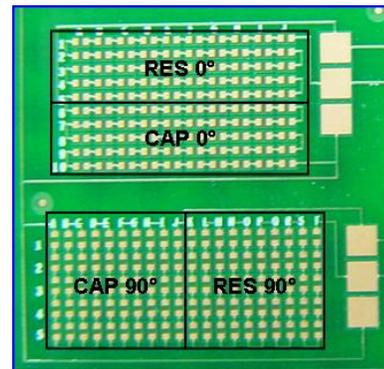


Figure 2. Individual test cell. Each test cell has 50 capacitors and resistors oriented at 0° and 50 of each component type oriented at 90°.

Stencil Design

To achieve all the combinations of aperture reductions and offsets in a single print, the following modifications were made to the stencil design. Moving left to right, of the six columns of test cells, the first two columns had apertures reduced to 70% of their pad area, the middle two columns were not populated, and the last two columns had no aperture reductions applied. Within each group of aperture reductions the test cells were divided into 4 segments, with each segment having a different aperture alignment offset.

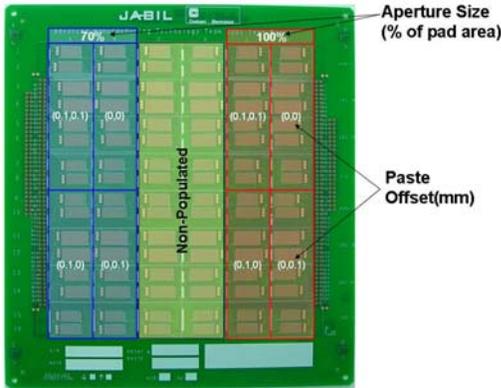


Figure 3. Stencil design modifications

Using the design shown in Figure 3, each combination of padstack design, aperture reduction, and alignment offset appears twice per board. Two replicates were used, so each combination was assembled in four test cells.

ASSEMBLY

Upon receipt of the components, samples were inspected, which included dimensional measurements and XRF screening to insure lead was not present in the system.

All test vehicles were assembled in the Advanced Manufacturing Technology laboratory of Jabil Circuit in St. Petersburg, FL using the following equipment:

- MPM Ultraprint 3000 stencil printer
- Koh Young KY3030-VAL paste measurement system
- Fuji AIM pick and place
- Vitronics-Soltec XPM² reflow oven
- Vi Technology Vi3K² automated optical inspection
- Phoenix Nanomex X-ray inspection

Details of the assembly process development are described below.

Stencil Printing

The investigation included high and low paste volume settings. In order to achieve two levels of paste volume, the stencil apertures were reduced. To identify the most appropriate aperture reduction, a prescreening study was performed. Stencil apertures were sized at 100%, 80% and 60% of their corresponding pad areas for all four footprints. It was determined through the prescreening DOE that 70% pad area, or 30% reduction, would be appropriate for the low setting. 100% pad area and 70% pad area equate to transfer efficiencies of roughly 60% and 50% respectively, and varied slightly with the individual solder pastes and aperture designs.

The stencils used in the study were electroformed nickel with 125 micron (5 mil) foils. All solder pastes were printed at the same parameters: 2 inch/sec squeegee speed, 1.25 lb/in squeegee pressure, slow separation speed.

Paste Volume Measurement

The Koh Young KY-3030VAL solder paste inspection system was used to measure paste volume deposition in all phases of the experiment. This proved to be especially useful in the pre-screening experiment to determine the appropriate aperture reduction to apply to the stencil design.

The equipment employs a proprietary Phase Shift Profilometry (PSP) algorithm using a moiré light projection technique. This technique uses opposing dual source LED lighting to capture 8 images (4 from each side) for every solder deposit. Using a reconstruction algorithm, the 8 images are combined to form a 3D model of the solder deposit. The dual source lighting technique is advantageous because it reduces the shadowing effect associated with single light source systems. With a pixel size of approximately 20um x 20um, it is very important to have the most accurate information possible, particularly with the 0201 deposits in the size range of 10-19 mils.

To ensure system capability, a rotational Gage R&R was performed using Minitab's crossed ANOVA method. The Total Gage R&R figure needs to be below 30 in order for the system to be used as an acceptable measurement instrument. Using a process tolerance window of +/-25%, the Total GRR for the test vehicle was around 20, with a repeatability figure below 3.

The cycle time for the equipment to measure nearly 20,000 solder deposits was approximately 55 seconds.

Placement

The Fuji AIM board assembler is a two gantry, 4 head placement machine that handles devices from 0201s to 74 mm square. It has 180 feeder inputs and can feed from tape and reel, strip tape, sticks, and matrix trays. Its speed is rated at 20,300 chips per hour.

The machine was installed in the laboratory and calibrated prior to the test. A GR&R study was not performed prior to the test.

Reflow Soldering

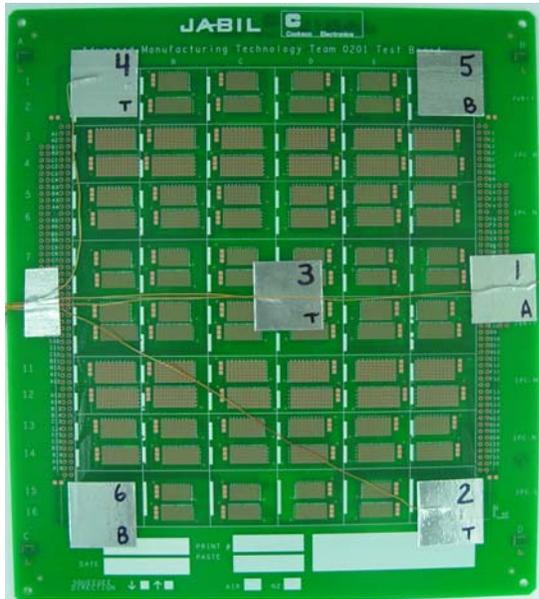


Figure 4. Thermocouple attachment. Locations 1 though 4 are on the top side; 5 and 6 are on the bottom side.

Six thermocouples were used to profile the assembly. Four were attached to the top side; two were attached to the bottom side as shown in Figure 4.

The reflow profiles depicted in Figure 5 through Figure 8 were developed on unpopulated PWBs.

SnPb Straight Ramp Profile



1.5 C/s ramp, 220 C peak, 50-60 sec above 183 C

Figure 5. Straight ramp profile, tin-lead

SnPb High Soak Profile



75 sec at 150 C, 220 C peak, 75 sec above 183 C

Figure 6. High soak profile, tin-lead

Pb-Free Straight Ramp Profile



1.5 C/s ramp, 245 C peak, 60-70 sec above 221 C

Figure 7. Straight ramp profile, SAC 305

Pb-Free High Soak Profile



60 sec at 175 C, 240 C peak, 60-70 sec above 221 C

Figure 8. High soak profile, SAC 305

Automated Optical Inspection

The Vi Technologies Vi3K2 AOI system was used to inspect boards pre- and post-reflow. Starting from the same CAD information, both programs were generated using the equipment manufacturer's standard library. The machine combines high end optics and hardware with software technologies such as vectoral imaging and sub-pixelization to provide accuracy and repeatability that allows Automated Optical Measurement (AOM). In the data presented below, the system was used to detect full and partial tombstones, and positional errors in X, Y, and theta. For this test, the equipment was installed and calibrated by the manufacturer; a GR&R study was not performed prior to the execution of the experiment.

X-Ray Inspection

The Phoenix Nanmoex X-ray machine was used to inspect for solder balls. PWBs were X-rayed, the resulting images were visually interpreted, and the solder ball count was manually recorded for each quadrant of the PWB. Solder ball defects were recorded for each PWB, but not uniquely associated with individual components.

DATA COLLECTION

Defects were classified as:

- Full tombstones, where the component stands completely up on one end at approximately a 90 degree angle to the plane of the PWB.
- Partial tombstones, also known as drawbridges, where the component is soldered at one termination but not at the other and stands at an angle between 0 and 90 degrees to the plane of the PWB
- Non-wets, where the component remains planar to the board surface, but the solder has not adequately wetted to one or both of the terminations.
- Positional errors, where one or both component terminations are offset from the edge of the pad by greater than 50% of the termination width in x, y, or theta.
- Solder balls, or spheres of solder that remain after the soldering process. The minimum size recorded was that which was visually perceptible on X-ray images, approximately 75 to 100 microns (3-4 mils) in diameter. Workmanship criteria such as locations relative to the components or levels of encapsulation were not recorded.

Examples of the defect modes are depicted in Appendix A.

RESULTS & DISCUSSION – Phase I Data

Defect Overview

Defect rates for six specific failure modes were recorded. The overall defect rate for the experiment was 11,823 ppm. The breakdown of the defects is shown in Figure 9.

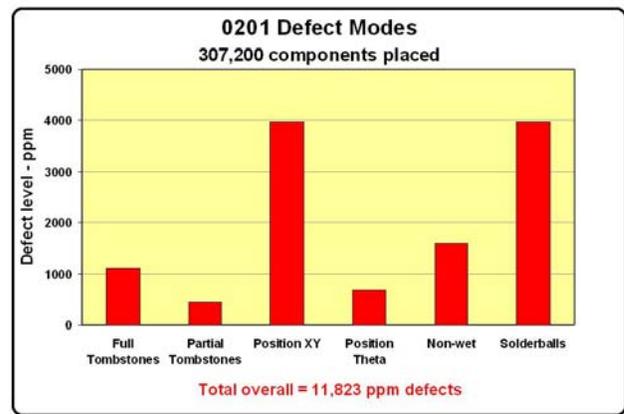


Figure 9. Distribution of all defects

Solder balls were the most commonly observed phenomena, but it should be noted that although they are all reported as defects in this study, not all the solder balls that were observed would necessarily represent defects in a production environment. Some of the solder balls observed would be considered defects and others would not. For example, solder balls that are larger than the minimum spacing of the SMT leads and are not entrapped or encapsulated enough (by no-clean flux residue) to prevent them from dislodging in their service environments would be considered defects. Solder balls that do not violate minimum spacing requirements or those judged to be adequately entrapped would not. Inspection criteria varies by product, but in general, solder ball formation is indicative of coalescence properties during reflow. Because solder balls showed such a considerable response in the experiment but workmanship standards vary widely, defect rates are reported with and without the inclusion of solder balls. When reviewing the results, solder balls should not be considered as absolute defects, but as relative indicators of coalescence.

Positional errors in the X and Y directions were observed with the same frequency as solder balls. The other failure modes observed (in order of declining frequency) were non-wets, full tombstones, and partial tombstones. Although these five failure modes were differentiated for the purposes of this investigation, from a production perspective they share a common characteristic: they all require rework.

Tombstone formation was the focus of the study; the data was statistically analyzed for the input variables' effect(s) on tombstoning rates. The top four contributors to tombstoning included three main effects and one interaction. The interaction between paste offset in the X direction and placement offset (in both X and Y) had the largest overall effect on tombstoning rates. When the effects of paste and placement offsets were removed, the overall defect rate dropped from 11,823 ppm to 2,513 ppm including the solder balls, or from 7,845 ppm to 156 ppm excluding the solder balls. The dramatic drop in all defect rates is shown in Figure 10.

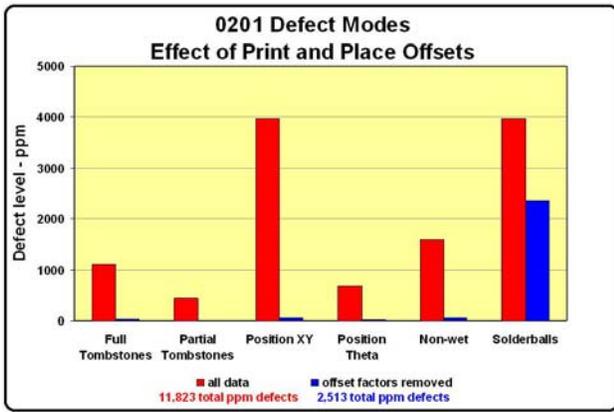


Figure 10. Effect of Offsets. The combination of paste offsets in the X direction and placement offsets in the X and Y direction were the main contributors to defects.

It is clear that eliminating unnecessary offsets in the printing and placement processes removes an enormous source of defect generation not only for tombstones, but for all defect modes. The placement offsets used in this study were representative of conditions that can commonly be found in an out of control production environment. The 0.1mm (4 mil) offset on placement coordinates is considered to be within the actual placement capability of many high-speed chip placement machines. Although the paste offset of 0.1mm (4 mil) is larger than the typical positional error on most stencil printers, the source of mis-registration between PWBs and stencils is typically not due to the equipment, but to either poor setup, or to alignment issues created by dimensional inaccuracy of the PWB or stencil.

It should be noted that the equipment used in these experiments were subject to their manufacturers' regular calibration procedures with no special tuning. GR&R studies were not performed on the printer or placement machine prior to the execution of the tests. The actual print alignment and placement accuracy are assumed to be within the manufacturer's specifications and exhibit typical positional drift from their programmed positions within these specifications.

Two placement offset cases were studied: nominal (0,0) and +0.1mm (4 mil) in both X and Y directions concurrently (+0.1, +0.1). Placement offsets were not subdivided into individual axis shifts (0,+0.1) and (+0.1,0), but print alignment offsets were performed with all four combinations. The combination of paste offset in X with placement offset had a tremendous effect on defects, but the combination of paste offset in Y with placement offset did not. The offset in X was in the positive direction, which is also the leading edge of the device as it enters the reflow zone. The effect witnessed here is likely similar to the effect of component orientation. Note that offsets were not tested in opposing directions, i.e. paste in negative X and placement in positive X and Y or vice versa, but it is assumed that it would hurt the tombstoning rates rather than help them.

The remainder of the variables that exhibited large influences on tombstoning were singular or main effects, and not as dramatic as the combined effect of the paste and placement offsets. The second most influential factor was component type. Capacitors exhibited a defect rate of 15,996 ppm (14,316 ppm excluding solder balls), while resistors exhibited a defect rate of 7,650 ppm (1,374 ppm excluding solder balls), as shown in Figure 11.

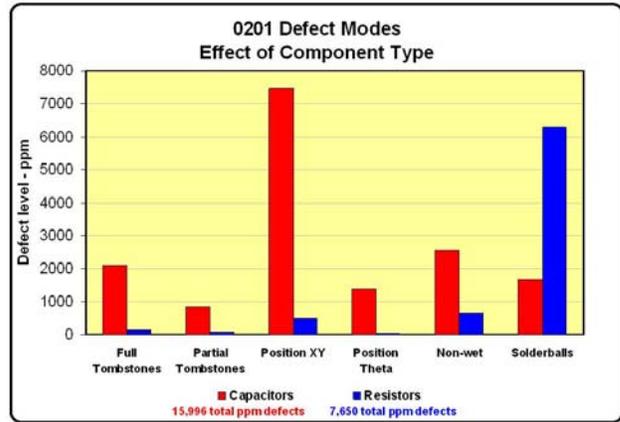


Figure 11. Effect of component type

Component Dimensions

	Comp Type	X	Y	Z	Lead length	Lead width
mm	C	0.27	0.53	0.26	0.12	0.26
	R	0.26	0.58	0.21	0.15	0.27
mils	C	10.8	21.1	10.3	4.8	10.2
	R	10.3	22.7	8.2	5.9	10.6

Table 2. 0201 component dimensions. Ten of each component type were measured and average values are shown.

Capacitors consistently showed higher defect rates in all categories except solder balls. The main differences between capacitors and resistors are their heights and termination geometries. The capacitors are 25% taller than resistors, and have a higher center of gravity, which can make them more likely to yield to the wetting forces that cause tombstones.

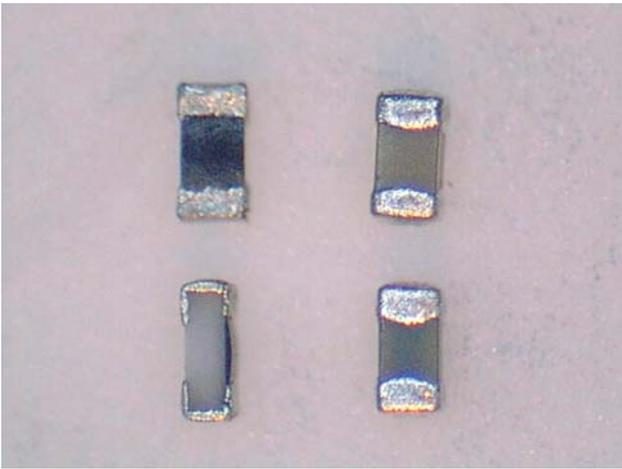


Figure 12. 0201 resistors (left) and capacitors (right).

Resistors showed three times the solder ball rate of capacitors. Regardless of whether or not certain solder balls are considered defects, the fact that resistors showed 3X higher incidence rate indicate that they are more susceptible to coalescence issues and solder balling defect modes, likely due to their 3-sided termination design, which has less surface area to draw molten solder than similarly sized capacitors (figure 12).

The third most predominant effect was that of orientation. Components oriented at 0 degrees, or parallel to the direction of travel through the oven, exhibited a defect rate of 15,046 ppm (11,699 ppm excluding solder balls), while components oriented at 90 degrees, or perpendicular to the direction of travel, exhibited a defect rate of 8600 ppm (3,991 ppm excluding solder balls). The results are shown in Figure 13.

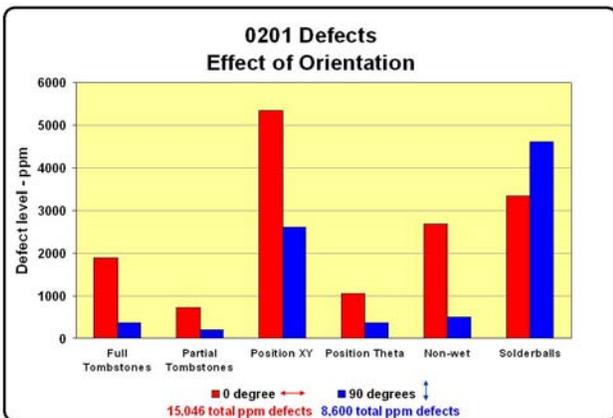


Figure 13. Effect of component orientation

The components oriented perpendicular to the direction of travel showed much fewer defects than those oriented parallel to the direction of travel, presumably due to thermal gradients across the component. When a component is oriented at 90 degrees, both terminations enter reflow at approximately the same time. When a component is oriented at 0 degrees, the leading termination enters reflow before the trailing termination.

The paste offset in the positive X direction was 0.1 mm (4 mils). Similar paste offsets in the Y direction did not show a significant impact on defect rates. This behavior may be similar to, or exacerbating the effect of, component orientation on the time differential reaching reflow temperatures.

The fourth largest effect was that of reflow atmosphere. Overall, air atmospheres were associated with defect rates of 18,581 ppm (11,172 ppm excluding solder balls); while the inert environments were associated with 5,065 ppm (4,518 ppm excluding solder balls). The results, shown in Figure 14, are split. Nitrogen environments produced more tombstone defects, but less positional and wetting defects. The nitrogen environment also minimized the formation of solder balls when compared to air, indicating improved coalescence. Overall, nitrogen environments produced fewer defects than air, but the impact on total defect reduction was not as large as the one provided by print and placement controls.

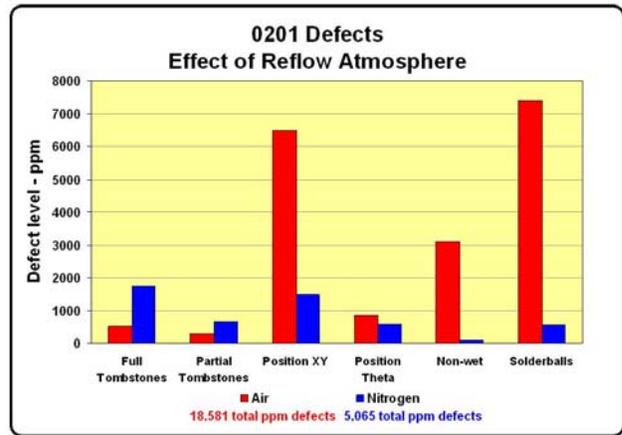


Figure 14. Effect of Atmosphere

Effect of Solder Paste Type

Figure 15 shows the defect rates for each solder paste type.

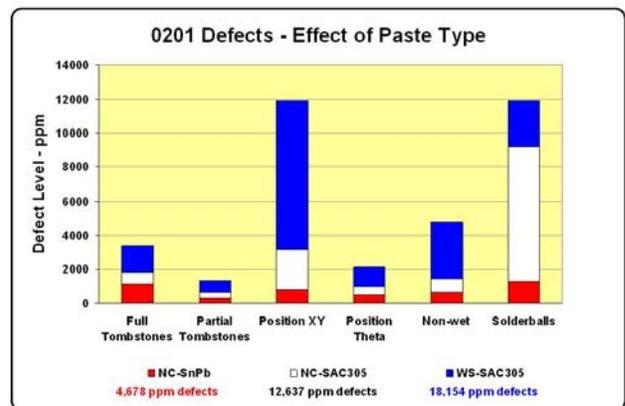


Figure 15. Effect of paste type on defect modes

Of the three paste types, the no-clean tin-lead paste produced the fewest overall defects, a total of 4,768 ppm

(3,679 excluding solder balls). The no-clean lead-free paste more than doubled that defect rate with 12,637 ppm (4,697 excluding solder balls). Solder balls were the most common issue for this paste, accounting for almost two-thirds of the recorded defects. Excluding the solder ball count, the defect rates for no-clean tin-lead and lead-free were not extremely different. The water soluble lead-free paste had the highest defect rate at 18,154 ppm (15,459 excluding solder balls).

When the key factors of print and placement offsets are removed, the defect rate drops dramatically for all paste types, as shown in Figure 16.

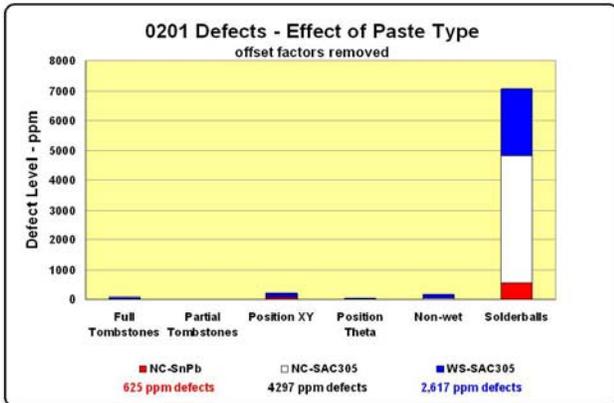


Figure 16. Effect of paste type on defect rates for process without print and placement offsets.

The defect rates for no-clean SnPb, no-clean SAC305 and water washable SAC305 drop to 625 ppm, 4,297 ppm, and 2,617 ppm respectively. Again, the vast majority of the recorded defects are solder balls; excluding them from the calculations reveals defect rates of 78 ppm, 39 ppm, and 352 ppm for each type of solder paste, averaging 156 ppm overall. Regardless of how the data is analyzed, the positive effect of controlling the print and placement process cannot be overlooked.

Effect of Padstack

Of the four different padstacks used in the experiment, three were suggested by IPC-7351. Their designations and dimensions are shown in Table 3

Designation	Pad Size
IPC – M	0.5mm x 0.5mm; 19.7 mils x 19.7 mils
IPC – N	0.4mm x 0.4mm; 15.7 mils x 15.7 mils
IPC – L	0.3mm x 0.3mm; 11.8 mils x 11.8 mils

Table 3. Pad sizes used in Phase 1 DOE.

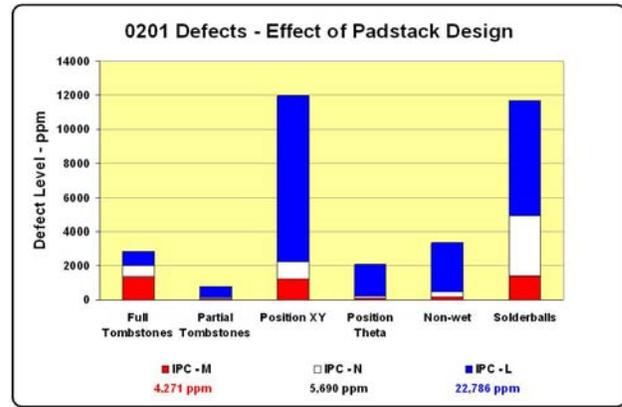


Figure 17. Effect of Padstack on defect rates

The padstack results are shown in Figure 17. The largest footprint, IPC-M, gave the least amount of defects, 4,271 ppm (2,904 excluding solder balls). The medium-sized footprint, IPC-N, showed higher overall defect rate, 5,690 ppm, but excluding the solder balls, it actually performed slightly better than the larger one, at 2,161 ppm. Given that the main purpose of using 0201 sized components is to more densely populate the PWB, the medium-sized footprint may be the better choice when deciding the trade-off between design functionality and manufacturability. The smallest padstack demonstrated the highest defect rate at 22,786 ppm (16,003 excluding solder balls).

CONCLUSION

The conditions that were varied in this phase of the experiment were component type, padstack, paste volume, paste offset, placement offset, reflow profile and reflow atmosphere.

The largest contributor to defect generation was the combination of 0.1 mm (4 mil) paste offsets in the X direction and concurrent 0.1 mm placement offsets in X and Y directions. In descending order of influence, the next three major factors were component type, orientation, and reflow atmosphere.

Of the top four factors, two cannot be controlled by the assembler. Component type and orientation are characteristics of the circuit design that are not likely to be changed. The reflow atmosphere may or may not be controllable, as the availability of nitrogen is limited by geographic location and cost sensitivity of the end product. The most predominant factor, however – the print and placement offsets – are almost completely controllable at the assembly level. The impact of removing mechanical slop from the assembly process brought the overall defect rates from 11,823 to 2,513 ppm, or from 7,845 ppm to 156 ppm excluding the solder ball count.

Both offset conditions can be addressed with ordinary process control methods. Machine repeatability can be measured through capability studies, positional accuracy can be addressed by calibration, and stencils/placement

programs can be scaled to compensate for the positional inaccuracies of the PWBs. It is a well accepted notion that process control improves yield performance, and that as feature sizes get smaller, controlling key parameters becomes increasingly important. The dramatic effect of the simulated “sloppy” print/place process on *all* defect modes demonstrates the necessity for process controls.

Of the three paste types, the no-clean tin-lead produced the least amount of overall defects, followed by no-clean lead-free and water washable lead-free. Under controlled print and placement conditions, both no-clean pastes produced defect levels of less than 100 ppm, regardless of atmosphere, profile, or padstack.

Of the four pad stacks, the largest produced the least defects, with the mid-sized pads running a close second. The smallest pad showed over 4 times as many defects as the largest or mid-sized pads.

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The following papers were used as reference documents in the design phase of the experiment:

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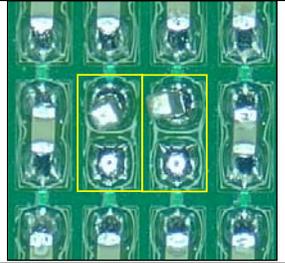
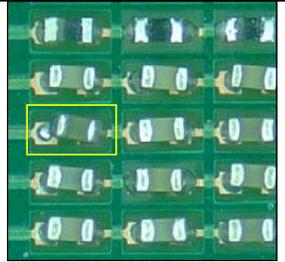
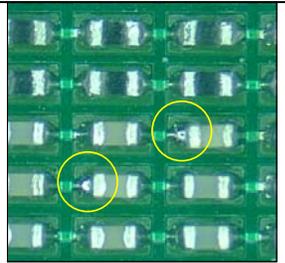
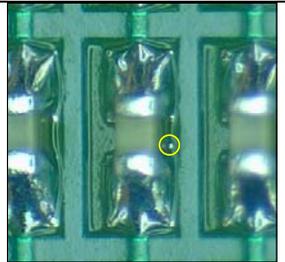
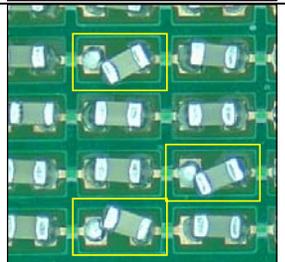
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APPENDIX A
Chip Component Defects Recorded in Study

Full Tombstone	 A micrograph showing a grid of chip components. Two components in the second row from the top are highlighted with yellow boxes, showing a full tombstone defect where the component is completely upright and not soldered to the board.
Partial Tombstone Or Drawbridge	 A micrograph showing a grid of chip components. One component in the second row from the top is highlighted with a yellow box, showing a partial tombstone or drawbridge defect where the component is partially upright and not fully soldered.
Non-wets	 A micrograph showing a grid of chip components. Two components in the second row from the top are highlighted with yellow circles, showing non-wet defects where the solder joints are incomplete or missing.
Solder Balls	 A micrograph showing a grid of chip components. A small yellow circle highlights a solder ball defect on a component in the second row from the top.
Position X-Y	 A micrograph showing a grid of chip components. A yellow box highlights a component in the second row from the top that is misaligned in its X-Y position.
Position Theta	 A micrograph showing a grid of chip components. Three components in the second row from the top are highlighted with yellow boxes, showing position theta defects where the components are rotated at an angle.

